Claims

[c1] A method of forming an integrated semiconductor structure comprising the steps of:

providing a semiconductor substrate that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and

fabricating at least one PFET and at least one NFET on the semiconductor substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction.

[c2] The method of Claim 1 wherein said at least one PFET and at least one NFET are formed by the steps of: forming a gate dielectric on a surface of the semiconductor substrate; forming patterned gate conductors on the gate dielectric; blocking some of the patterned gate conductors with a block mask; forming source/drain regions in the unblocked areas; removing the block mask; forming another block mask over areas containing the source and drain regions; and forming source/drain regions in the previously unblocked areas.

[c3] The method of Claim 2 further comprising forming spacers on exposed sidewalls of each patterned gate conductor prior to said blocking step.

[c4] The method of Claim 2 wherein said gate dielectric is formed by a thermal process or deposition.

[c5] The method of Claim 2 wherein the patterned gate conductors are formed by deposition and etching.

[c6] The method of Claim 1 wherein the at least one NFET comprises source/drain regions formed by ion implanting a dopant selected from the group consisting of arsenic and phosphorus into the semiconductor substrate.

[c7] The method of Claim 1 wherein the at least one PFET comprising source/drain regions formed by ion implanting a dopant selected from the group consisting of boron and antimony into the semiconductor substrate.

[c8] The method of Claim 1 wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.

[c9] The method of Claim 1 wherein said fabricating comprises placing the at least one PFET such that the current flow of the at least one PFET is pointed to the notch.

[c10] The method of Claim 1 wherein said fabricating comprises placing the at least one NFET such that the current flow of the at least one NFET is perpendicular to the notch.

[c11] An integrated semiconductor structure comprising a semiconductor substrate that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and at least one PFET and at least one NFET located on the semiconductor substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction.

[c12] The integrated semiconductor structure of Claim 11 wherein said semiconductor structure is a semiconducting material selected from the group consisting of Si, SiGe, SiC, SiGeC, GaAs, InAs, InP and other like III/V compound semiconductors.

[c13] The integrated semiconductor structure of Claim 12 wherein the semiconductor material is Si.

[c14] The integrated semiconductor structure of Claim 11 wherein the at least one NFET and the at least one PFET each comprise a gate dielectric located on the semiconductor substrate, a patterned gate conductor located on portions of the gate dielectric, and spacers located on exposed sidewalls of the patterned gate conductor.

[c15] The integrated semiconductor structure of Claim 14 wherein the gate dielectric is an oxide.

[c16] The integrated semiconductor structure of Claim 14 wherein the patterned gate conductor comprises polySi.

[c17] The integrated semiconductor structure of Claim 11 wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.